Attorney Docket # 5367-223PUS Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of Dominik EISERT et al. Serial No.: 10/572,655 Filed: March 6, 2007 For: Radiation-Emitting Thin-Film Semiconductor Chip	Examiner: LAM, Cathy N. Group Art: 2811

Commissioner for Patents
Alexandria, VA 22313-1450

APPEAL BRIEF

SIR:

This is an appeal, pursuant to 37 C.F.R. § 41.37, from the decision of the Examiner in the above-identified application, as set forth in the Final Office Action dated June 29, 2010 wherein the Examiner finally rejected Appellants' claims. The rejected claims are reproduced in the Appendix A attached hereto. A Notice of Appeal was filed on September 24, 2010 together with a Pre-Appeal Brief Request For Review. A Panel Decision was issued on October 27, 2010.

Please charge the amount of $540 in payment of the government fee for filing an Appeal Brief pursuant to 37 C.F.R. § 41.20 to our PTO Deposit Account No. 03-2412.

Appellants hereby petition for a one-month extension based on the mail date of Panel Decision issued October 27, 2010. Please charge our PTO Deposit Account No. 03-2412 in the amount of $110.00 in payment of the government fee for a one-month extension of time so that the period for response is extended to December 27, 2010.

Any additional fees or charges in connection with this application may be charged to our PTO Deposit Account No. 03-2412.

REAL PARTY IN INTEREST

The assignee, Osram Opto Semiconductors GmbH, of applicant, Dominik EISERT et al., is the real party of interest in the above-identified U.S. Patent Application.

RELATED APPEALS AND INTERFERENCES

There are no other appeals and/or interferences related to the above-identified application at the present time.

STATUS OF CLAIMS

Claims 1-2, 4-8, 10-18, and 44-73 are pending in the subject application with claims 1 and 46 being the only independent claims.

Claims 3 and 9 have been previously cancelled without prejudice or disclaimer. Claims 19-43 have been cancelled in view of the Restriction Requirement.

Claims 1-2, 4-8, 10-18, and 44-73 have been rejected and are on appeal.

STATUS OF AMENDMENTS

There have been no Amendments filed subsequent to the Final Office Action.

SUMMARY OF THE CLAIMED SUBJECT MATTER

The following descriptive details are based on the specification. They are provided only for the convenience of the Board as part of the discussion presented herein, and are not intended to argue limitations which are unclaimed. The page and line numbers referred to in this section correspond to those of appellants' specification as filed.

Appellants' invention is directed to a radiation-emitting thin-film semiconductor chip (10), as is generally shown Fig. 1 of the subject application (Fig. 1 is reproduced below for the Board's convenient reference):

FIG 1

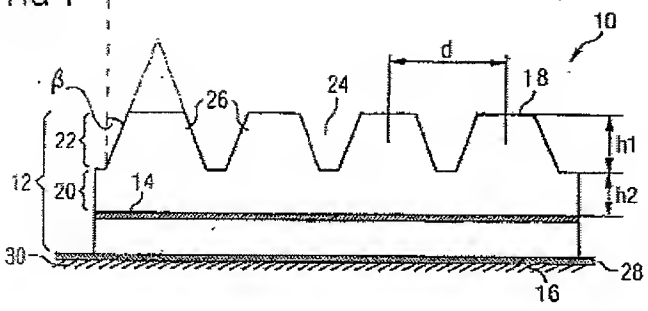
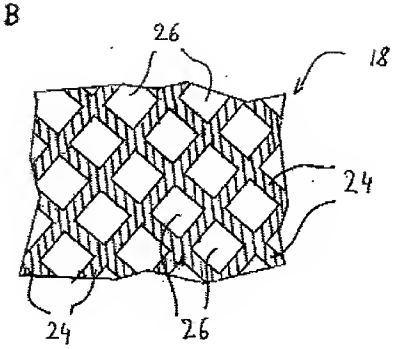


FIG 9B



The radiation-emitting thin-film semiconductor chip (10) comprises an epitaxial multilayer structure (12) (see pg. 10, ll. 15-16) and a reflective layer or interface (28) (see pg. 11, ll. 1-2). The epitaxial multilayer structure (12) comprises an active, radiation-generating layer (14) (see pg. 10, ll. 16-18), a first main face (16), and a second main face (18) remote from the first main face (16) for coupling out radiation generated in the active, radiation-generating layer (14) (see pg. 10, ll. 23-26). The first main face (16) of the multilayer structure (12) is coupled to the reflective layer or interface (28) (see Fig. 1).

The epitaxial multilayer structure (12) also has a patterned region (22) that adjoins the second main face (18) of the multilayer structure (12) (see pg. 11, ll. 18-21). The patterned region (22) comprises convex elevations (26) (see Fig. 1) defined by either one- or two-dimensional depressions (24) (see, pg. 11, ll. 29-36 and Figs. 1 and 9B reproduced above). In a first embodiment, the convex elevations (26) have a height (h1) at least as large as a distance (h2) between the patterned region (22) and the active, radiation-generating layer (14) (see pg. 13, ll. 27-29). In a second embodiment, the convex elevations (26) have an inclination angle (ß) of between approximately 30° and approximately 70° (see pg. 13, ll. 16-17).

GROUNDS OF REJECTION TO BE REVIEWED IN APPEAL

Whether claims 1-2, 4-8, 10-18, and 44-61 have been rejected under 35 U.S.C. §103(a) as being unpatentable over US 6,291,839 to Lester?

ARGUMENTS

A. Independent Claims 1 and 46 are Not Obvious Over Lester

Independent claims 1 and 46 each recite "a patterned region of the multilayer structure that adjoins the second main face of the multilayer structure is patterned by either one- or two-dimensional depressions forming convex elevations."

In rejecting independent claims 1 and 46, the Examiner asserts that Lester's layer 16 is patterned by one- or two- dimensional depressions forming truncated pyramids (see bottom of page 2 of the final Office Action). Appellants disagree.

Lester teaches a light emitting device (LED) having a finely-patterned reflective contact. In the Examiner-cited portions, Lester explicitly teaches that:

> FIG. 5 illustrates another preferred embodiment. The top surface of the LED has been roughened, preferably in alignment with the openings in the contact. This may be achieved by etching the GaN in a self-aligned fashion during the same lithographic step used to pattern the contact. The etched holes can extend into the p-layer 16 or can be etched as deep as the substrate 8. (See col. 5, ll. 8-14 of Lester; emphasis added.)

In light of the explicit teachings by Lester, one skilled in the art will appreciate that Lester merely teaches forming etched holes in a continuous layer 16. When such etched holes were viewed in a top down direction with the contact 20 removed, they are likely to resemble a pattern similar to the finely spaced pattern of openings in the contact 20, as shown in Fig. 1 and disclosed in column 3, lines 1-3 of Lester.

There are neither one-dimensional nor two-dimensional depressions in Lester, much less ones "forming convex elevations" as recited in independent claims 1 and 46. If the finely spaced pattern of openings in Lester's contact 20 are considered as the claimed depressions, which appellants disagree, such finely spaced pattern of openings are neither one-dimensional nor two-dimensional, as are the claimed depressions recited in independent claims 1 and 46. Accordingly, Lester's structure clearly differs from those of the claimed invention.

To further illustrate the difference between the one- and two-dimensional depressions forming convex elevations as claimed and the structure taught by Lester, appellants produce below Figures A to C showing perspective views of the different structures according to the claimed invention and Lester:

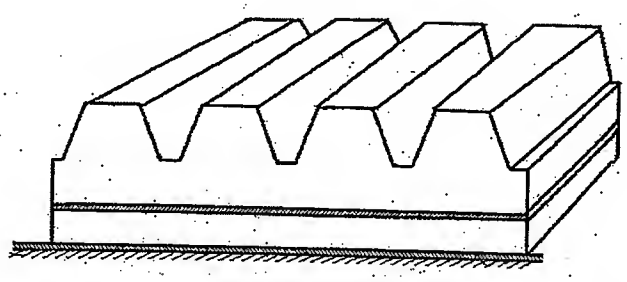


Figure A above shows one-dimensional depressions forming convex elevations as claimed

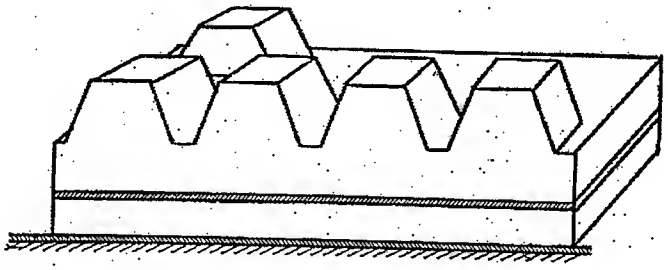


Figure B above shows two-dimensional depressions forming convex elevations as claimed

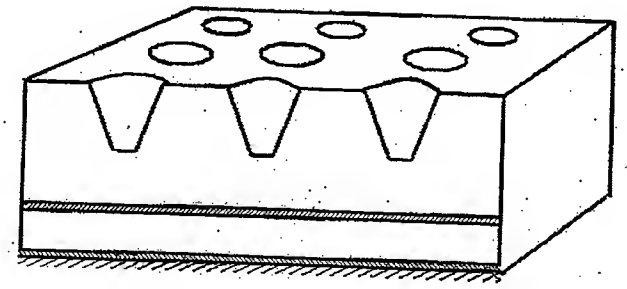


Figure C above shows the structure of Lester containing etched holes formed in a continuous layer

As it becomes clear from the above Figures A-C, all three structures illustrated have the same sectional view. Nevertheless, the structure taught by Lester (Figure C) clearly differs from

those of the claimed invention (Figures A and B). More specifically, Lester's structure contains concave etched holes formed in the p-type layer 16 (see, also, Fig. 5 of Lester), rather than convex elevations formed by one- and two-dimensional depressions expressly recited in independent claims 1 and 46.

In the Office Action, the Examiner incorrectly interprets Fig. 5 of Lester to show convex elevations (see pg. 2 of the Office Action). Fig. 5 of Lester shows a sectional view of such etched holes in Lester's LED device and cannot be interpreted to show either one- and two-dimensional depressions or convex elevations, as asserted in the Office Action. Accordingly, Lester does not teach the above recited features of independent claims 1 and 46.

Moreover, Lester's layer 20 with etched holes is a current-spreading layer used to spread the current for driving Lester's device over the entire p-side (see, e.g., col. 3, ll. 11-15 or col. 2, ll. 18-23 of Lester). Consequently, one skilled in the art would not modify the etched holes of Lester to one- or two-dimensional depressions forming convex elevations as such elevations would not allow for a continuous layer 20 necessary for spreading current impressed by p-contact pad 21 over the entire p-side (see Fig. 1 of Lester) and thus render Lester inoperable. Therefore, the above-recited features of independent claims 1 and 46 are not obvious over Lester.

In the "Response to Arguments" section of the Final Office Action, the Examiner states that Fig. 5 of Lester teaches the above-recited claim features of independent claims 1 and 46 based on the findings that the cross sectional view in Lester (i.e., Fig. 5) is not different from the cross sectional view of the claimed invention of Fig. 1 (see item no. 4 in Office Action). Applicants disagree and assert that the Examiner's findings are inadequate to support the above conclusion. The mere fact that two objects have the same cross-section does not necessarily mean they have the same structure. For example, both a ball and circular cylinder can have a circular cross-sectional shape, but are of different structures. Therefore, the similar cross

sectional shapes in Fig. 5 of Lester and Fig. 1 of the subject application do not suggest that Lester teaches the above-recited claim features of independent claims 1 and 46.

Indeed, Fig. 5 of Lester depicts only a sectional view of the LED and shows the etched holes formed into the p-type layer 16. As stated above, the top surface of Lester's LED has been roughened to align with the openings in the contact by etching the GaN (see, e.g., col. 5, ll. 10-12 of Lester). The formation of the etched holes in Lester does not result in a patterned region having multiple convex elevations as recited in independent claims 1 and 46. Instead, the p-type layer 16 of Lester has a single elevation (the continuous region surrounding the holes).

With respect to the Examiner's response to applicants' previous arguments concerning the continuous layer 20 necessary for spreading current over the entire p-side (see page 13 of the Office Action), applicants clarify that such arguments are intended and proper to prove lack of motivation to modify Lester's etched holes to arrive at the claimed one- or two-dimensional depressions.

In view of the foregoing, independent claims 1 and 46 each patentably distinguish over Lester. The 35 U.S.C. § 103(a) rejections of independent claims 1 and 46, as well as the dependent claims, should be reversed.

B. Dependent Claim 62 is not Obvious over Lester for Additional Reasons

Claim 62 recites that "the second main face is a noncontinuous layer." In contrast, the second main face of Lester's device is a continuous layer (see Figure C of the enclosed illustration). Therefore, Lester does not teach or suggest the above-recited claim features of claim 62.

Claim 62 thus patentably distinguishes over Lester and is allowable for the above additional reasons.

CONCLUSION

For the foregoing reasons, it is respectfully submitted that Appellants' claims are not rendered obvious by the cited prior art and are, therefore, patentable over the art of record, and that the Examiner's rejections should be reversed.

Respectfully submitted,
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CLAIMS APPENDIX

1. (Previously Presented) A radiation-emitting thin-film semiconductor chip comprising:

an epitaxial multilayer structure comprising:

an active, radiation-generating layer,

a first main face, and

a second main face remote from the first main face for coupling out radiation generated in the active, radiation-generating layer, and

a reflective layer or interface,

wherein the first main face of the multilayer structure is coupled to the reflective layer or interface, and

wherein a patterned region of the multilayer structure that adjoins the second main face of the multilayer structure is patterned by either one- or two-dimensional depressions forming convex elevations, the convex elevations having a height (h1) at least as large as a distance (h2) between the patterned region and the active, radiation-generating layer.

2. (Previously Presented) The semiconductor chip as claimed in claim 1, further comprising a carrier element coupled to the first main face, wherein the reflective layer or interface is arranged between the carrier element and the multilayer structure.

3. (Cancelled).

4. (Previously Presented) The semiconductor chip as claimed in claim 1, wherein the elevations have a form of truncated pyramids or truncated cones or a trapezoidal cross-sectional form.

5. (Previously Presented) The semiconductor chip as claimed in claim 1, wherein the elevations have a form of cones or a triangular cross-sectional form.

6. (Previously Presented) The semiconductor chip as claimed in claim 1, wherein the elevations have a form of sphere segments or a circle segment cross-sectional form.

7. (Previously Presented) The semiconductor chip as claimed in claim 1, wherein the elevations have an inclination angle (β) of between approximately 30° and approximately 70°.

8. (Previously Presented) The semiconductor chip as claimed in claim 7, wherein the elevations have an inclination angle (β) of between approximately 40° and approximately 50°.

9. (Cancelled).

10. (Previously Presented) The semiconductor chip as claimed in claim 1, wherein the height (h1) of the elevations is approximately twice as large as the distance (h2) between the patterned region of the multilayer structure and the active, radiation-generating layer.

11. (Previously Presented) The semiconductor chip as claimed in claim 1, wherein a cell size (d) of the elevations is at most approximately five times as large as the height (h1) of the elevations.

12. (Previously Presented) The semiconductor chip as claimed in claim 11, wherein the cell size (d) of the elevations is at most approximately three times as large as the height (h1) of the elevations.

13. (Previously Presented) The semiconductor chip as claimed in claim 1, wherein the reflective layer or interface coupled to the first main area of the multilayer structure has a reflectivity of at least 70%.

14. (Previously Presented) The semiconductor chip as claimed in claim 1, wherein the reflective layer or interface coupled to the first main area of the multilayer structure has a reflectivity of at least 85%.

15. (Previously Presented) The semiconductor chip as claimed in claim 1, wherein the multilayer structure is applied onto a carrier substrate either directly by the first main face or via the reflective layer.

16. (Previously Presented) The semiconductor chip as claimed in claim 15, wherein the reflective layer or the carrier substrate serves as a contact layer of the semiconductor chip.

17. (Previously Presented) The semiconductor chip as claimed in claim 1, further comprising a conductive, transparent layer applied onto the second main face of the multilayer structure.

18. (Previously Presented) The semiconductor chip as claimed in claim 1, further comprising a transparent protective layer applied onto the second main face of the multilayer structure.

19-43. (Cancelled).

44. (Previously Presented) The semiconductor chip as claimed in claim 1, wherein each of the convex elevations is defined by two-dimensional depressions.

45. (Previously Presented) The semiconductor chip as claimed in claim 1, wherein the epitaxial multilayer structure of the semiconductor chip is free of a growth substrate.

46. (Previously Presented) A radiation-emitting thin-film semiconductor chip comprising an epitaxial multilayer structure and a reflective layer or interface, the epitaxial multilayer structure comprising:

an active, radiation-generating layer,

a first main face, and

a second main face remote from the first main face for coupling out the radiation generated in the active, radiation-generating layer,

wherein the first main face of the multilayer structure is coupled to the reflective layer or interface, and

wherein a patterned region of the multilayer structure that adjoins the second main face of the multilayer structure is patterned by either one- or two-dimensional depressions forming convex elevations, the convex elevations having an inclination angle (ß) of between approximately 30° and approximately 70°.

47. (Previously Presented) The semiconductor chip as claimed in claim 46, wherein the epitaxial multilayer structure of the semiconductor chip is free of a growth substrate.

48. (Previously Presented) The semiconductor chip as claimed in claim 46, further comprising a carrier element coupled to the first main face, wherein the reflective layer or interface is arranged between the carrier element and the multilayer structure.

49. (Previously Presented) The semiconductor chip as claimed in claim 46, wherein the elevations have a form of truncated pyramids or truncated cones or a trapezoidal cross-sectional form.

50. (Previously Presented) The semiconductor chip as claimed in claim 46, wherein the elevations have a form of cones or a triangular cross-sectional form.

51. (Previously Presented) The semiconductor chip as claimed in claim 46, wherein the elevations have an inclination angle (β) of between approximately 40° and approximately 50°.

52. (Previously Presented) The semiconductor chip as claimed in claim 46, wherein the elevations have a height (h1) at least as large as a distance (h2) between the patterned region and the active, radiation-generating layer.

53. (Previously Presented) The semiconductor chip as claimed in claim 52, wherein the height (h1) of the elevations is approximately twice as large as the distance (h2) between the patterned region and the active, radiation-generating layer.

54. (Previously Presented) The semiconductor chip as claimed in claim 46, wherein a cell size (d) of the elevations is at most approximately five times as large as a height (h1) of the elevations.

55. (Previously Presented) The semiconductor chip as claimed in claim 54, wherein the cell size (d) of the elevations is at most approximately three times as large as the height (h1) of the elevations.

56. (Previously Presented) The semiconductor chip as claimed in claim 46, wherein the reflective layer or interface coupled to the first main area of the multilayer structure has a reflectivity of at least 85%.

57. (Previously Presented) The semiconductor chip as claimed in claim 47, wherein the multilayer structure is applied onto a carrier substrate either directly by the first main face or via the reflective layer or interface.

58. (Previously Presented) The semiconductor chip as claimed in claim 57, wherein the reflective layer or interface or the carrier substrate serves as a contact layer of the semiconductor chip.

59. (Previously Presented) The semiconductor chip as claimed in claim 46, further comprising a conductive, transparent layer applied onto the second main face of the multilayer structure.

60. (Previously Presented) The semiconductor chip as claimed in claim 46, further comprising a transparent protective layer applied onto the second main face of the multilayer structure.

61. (Previously Presented) The semiconductor chip as claimed in claim 46, wherein the multilayer structure comprises a material or a plurality of different materials based on GaN.

62. (Previously Presented) The semiconductor chip as claimed in claim 1, wherein the second main face is a noncontinuous layer.

63. (Previously Presented) The semiconductor chip as claimed in claim 1, wherein the reflective layer is in direct contact with the epitaxial multilayer structure.

64. (Previously Presented) The semiconductor chip as claimed in claim 1, wherein the epitaxial multilayer structure is based on a II-VI semiconductor material.

65. (Previously Presented) The semiconductor chip as claimed in claim 1, wherein the epitaxial multilayer structure is based on a phosphide compound semiconductor material.

66. (Previously Presented) The semiconductor chip as claimed in claim 1, wherein the epitaxial multilayer structure is based on an arsenide compound semiconductor material.

67. (Previously Presented) The semiconductor chip as claimed in claim 1, wherein the patterned region of the multilayer structure that adjoins the second main face of the multilayer structure is patterned by two-dimensional depressions forming convex elevations.

68. (Previously Presented) The semiconductor chip as claimed in claim 46, wherein the second main face is a noncontinuous layer.

69. (New) The semiconductor chip as claimed in claim 46, wherein the reflective layer is in direct contact with the epitaxial multilayer structure.

70. (Previously Presented) The semiconductor chip as claimed in claim 46, wherein the epitaxial multilayer structure is based on a II-VI semiconductor material.

71. (Previously Presented) The semiconductor chip as claimed in claim 46, wherein the epitaxial multilayer structure is based on a phosphide compound semiconductor material.

72. (Previously Presented) The semiconductor chip as claimed in claim 46, wherein the epitaxial multilayer structure is based on an arsenide compound semiconductor material.

73. (Previously Presented) The semiconductor chip as claimed in claim 46, wherein the patterned region of the multilayer structure that adjoins the second main face of the multilayer structure is patterned by two-dimensional depressions forming convex elevations.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.